REMARKS

Claims 13 and 22 are objected to under 37 C.F.R. 1.75(c). Claims 13 and 22 are amended to recite that the nickel silicide layer is the nickel alloy silicide layer, the nickel alloy silicide layer containing at least one material selected from the group consisting of tantalum (Ta), zirconium (Zr), titanium (Ti), hafnium (Hf), tungsten (W), cobalt (Co), platinum (Pt), molybdenum (Mo), palladium (Pd), vanadium (V) and niobium (Nb). It is believed that, with these amendments and the amendments to claims 12 and 21, all of the objections are overcome. Reconsideration is requested.

Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffmann, *et al.* (U.S. Publication Number 2004/0253776). Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffmann, *et al.* in view of Brown, *et al.* (U.S. Patent Number 5,264,724). Claims 10-14 and 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffmann, *et al.* in view of Ito (U.S. Patent Number 6,656,853). Claims 15-18 and 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffmann, *et al.* in view of Ito and Brown, *et al.* In view of the amendments to the claims and following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-9, a method of fabricating a semiconductor device includes forming a stress layer on a source region, a drain region and a gate electrode. After forming the stress layer, the stress layer on the source region, the drain region and the gate electrode is annealed to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer.

Claims 1-9 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the method of fabricating the semiconductor device includes after forming the stress layer, annealing the stress layer on the source region, the drain region and the gate electrode to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 10-18, a method of fabricating a

semiconductor device includes forming a stress layer on a nickel silicide layer over a gate electrode and source and drain regions. After forming the stress layer, the stress layer over the gate electrode and the source and drain regions is annealed to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer.

Claims 10-18 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the method of fabricating the semiconductor device includes after forming the stress layer, annealing the stress layer over the gate electrode and the source and drain regions to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 19-27, a method of fabricating a semiconductor device includes forming a stress layer on a semiconductor substrate including a nickel silicide layer, forming a lower interlayer insulating layer on the stress layer, and patterning the lower interlayer insulating layer to selectively expose the stress layer over an active region. After patterning the lower interlayer insulating layer, the exposed stress layer is annealed to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer.

Claims 19-27 are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the method includes after patterning the lower interlayer insulating layer to selectively expose the stress layer, annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

Hoffmann, *et al.* discloses a silicon oxide straining layer 213 deposited on a silicon gate electrode 130. The silicon oxide straining layer 213 formed only on gate electrode 130 may be doped, and, optionally, a heating and/or annealing treatment may subsequently be performed.

With regard to the rejection of claims 1-5 as being anticipated by Hoffmann, *et al.*, Hoffmann, *et al.* fails to teach or suggest that a method includes after forming a stress layer,

annealing the stress layer on a source region, a drain region and a gate electrode to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 1-9. Instead, in Hoffmann, *et al.*, when the doped oxide straining layer 213 is annealed, the doped oxide straining layer 213 is only on the gate electrode, and is not over a source region, a drain region and a gate electrode, as claimed in claims 1-9.

Hoffmann, *et al.* fails to teach or suggest these elements of the invention set forth in claims 1-9. Specifically, Hoffmann, *et al.*, fails to teach or suggest that a method includes after forming a stress layer, annealing the stress layer on a source region, a drain region and a gate electrode to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 1-9. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-5 under 35 U.S.C. 102(e) as being anticipated by Hoffmann, *et al.*, is respectfully requested.

With regard to the rejection of claims 6-9 as being unpatentable over Hoffmann, *et al.* and Brown, *et al.*, Brown, *et al.* is cited in the Office Action as teaching a PECVD deposition method for silicon nitride at a temperature below 500°C to a thickness of 1000Å, and an annealing process between 400-500°C in an ambient nitrogen gas.

Brown, *et al.* fails to teach or suggest that a method includes after forming a stress layer, annealing the stress layer on a source region, a drain region and a gate electrode to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 1-9.

Brown, *et al.*, like Hoffmann, *et al.*, fails to teach or suggest these elements of the invention set forth in claims 1-9. Specifically, Brown, *et al.*, fails to teach or suggest that a method includes after forming a stress layer, annealing the stress layer on a source region, a drain region and a gate electrode to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 1-9. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 1-9. Therefore, it is believed that claims 1-9 are allowable over the cited references, and

reconsideration of the rejections of claims 6-9 under 35 U.S.C. § 103(a) based on Hoffmann, *et al.* and Brown, *et al.* is respectfully requested.

With regard to the rejection of claims 10-14 and 19-23 as being unpatentable over Hoffmann, *et al.* and Ito, Hoffmann, *et al.* fails to teach or suggest that a method of fabricating a semiconductor device includes after forming a stress layer, annealing the stress layer over a gate electrode and source and drain regions to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 10-18. Instead, in Hoffmann, *et al.*, when the doped oxide straining layer 213 is annealed, the doped oxide straining layer 213 is only on the gate electrode, and is not over a gate electrode and source and drain regions as claimed in claims 10-18. Hoffmann, *et al.* further fails to teach or suggest that a method includes after patterning a lower interlayer insulating layer to selectively expose a stress layer, annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer, as claimed in claims 19-27. Hoffmann, *et al.* does not teach a lower interlayer insulating layer, and therefore fails to teach or suggest after patterning a lower interlayer insulating layer to selectively expose a stress layer, annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer as claimed in claims 19-27.

Ito discloses depositing a silicon nitride layer 9 within a reactor chamber 40. After the deposition of the silicon nitride layer 9, a dielectric layer 10 is formed over silicon nitride layer 9. The dielectric layer 10 functions to maintain tensile stress created within the silicon nitride layer 9. Thus, the tensile stress in the silicon nitride layer 9 is formed during deposition of the silicon nitride layer 9. The dielectric layer 10 is etched to form etch-openings 12 and the silicon nitride layer is used as an etch stop. Silicon nitride layer 9 is then etched to form contact holes 12a. The silicon nitride layer 9 is not annealed after etching of dielectric layer 10.

Like Hoffmann, *et al.*, Ito fails to teach or suggest that a method of fabricating a semiconductor device includes after forming a stress layer, annealing the stress layer over a gate electrode and source and drain regions to convert a physical stress of the stress layer into a tensile

stress or increase a tensile stress of the stress layer, as claimed in claims 10-18. Instead, in Ito, the tensile stress in the silicon nitride layer 9 is formed during deposition of the silicon nitride layer 9 and the dielectric layer 10 is formed to maintain the tensile stress in silicon nitride layer 9. Ito does not anneal the silicon nitride layer 9 after it is formed, and because the tensile stress is formed during deposition there would be no motivation to anneal the silicon nitride layer 9. In addition, Ito fails to teach or suggest that a method includes after patterning a lower interlayer insulating layer to selectively expose a stress layer, annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer, as claimed in claims 19-27. Instead, in Ito, after the dielectric layer 10 is etched to form contact holes 12a, the silicon nitride layer 9 is not annealed.

Hoffmann, *et al.* and Ito fail to teach or suggest these elements of the invention set forth in claims 10-18 and 19-27. Specifically, Hoffmann, *et al.* and Ito fail to teach or suggest that a method of fabricating a semiconductor device includes after forming a stress layer, annealing the stress layer over a gate electrode and source and drain regions to convert a physical stress of the stress layer into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 10-18, and that a method includes after patterning a lower interlayer insulating layer to selectively expose a stress layer, annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer, as claimed in claims 19-27. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 10-18 and 19-27. Therefore, it is believed that claims 10-18 and 19-27 are allowable over the cited references, and reconsideration of the rejections of claims 10-14 and 19-23 under 35 U.S.C. § 103(a) based on Hoffmann, *et al.* and Ito is respectfully requested.

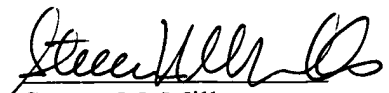
With regard to the rejection of claims 15-18 and 24-27 as being unpatentable over Hoffmann, *et al.*, Ito, and Brown, *et al.*, Brown, *et al.* fails to teach or suggest that a method of fabricating a semiconductor device includes after forming a stress layer, annealing the stress layer over a gate electrode and source and drain regions to convert a physical stress of the stress layer

into a tensile stress or increase a tensile stress of the stress layer, as claimed in claims 10-18. In addition, Brown, *et al.* fails to teach or suggest that a method includes after patterning a lower interlayer insulating layer to selectively expose a stress layer, annealing the exposed stress layer to convert a physical stress of the exposed stress layer into a tensile stress or increase a tensile stress of the exposed stress layer, as claimed in claims 19-27.

Brown, *et al.*, like Hoffmann, *et al.* and Ito, fails to teach or suggest these elements of the invention set forth in claims 10-18 and 19-27. Accordingly, there is no combination of the references which would provide such teaching or suggestion. None of the references, taken alone or in combination, teaches or suggests the invention set forth in claims 10-18 and 19-27. Therefore, it is believed that claims 10-18 and 19-27 are allowable over the cited references, and reconsideration of the rejections of claims 15-18 and 24-27 under 35 U.S.C. § 103(a) based on Hoffmann, *et al.*, Ito and Brown, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,



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